Sun™ Small Programmable Object Technology (Sun SPOT) Theory of Operation

Sun Labs

November 15, 2006

Sun Microsystems, Inc.
4150 Network Circle
Santa Clara, CA 95045 U.S.A.
650 960-1300

Revision 1.0.7, November 15, 2006

Sun™ Small Programmable Object Technology (Sun SPOT) Theory of Operation

---

This document describes the Sun Small Programmable Object Technology (SPOT) hardware platform. It describes

- the development kit contents
- the main board, the eSPOT hardware
- requirements for any eSPOT daughterboards
- the supplied daughterboard, the eDemo board

How to look at this draft:

This draft is written using the conditional text feature of FrameMaker.

I have created two classes of conditional text. One is for comments - that is communications from the writer to the reviewer. This paragraph has been labeled a comment. Comments are Magenta and underlined.

The other class of conditional text is "HideForCustomers." Text in this class is dark blue and underlined. It is intended to include information that we want to appear in the internal version of the document but not in the external version of the document. This paragraph has been labeled "HideForCustomers."

The only archane part of this process is the fact that FrameMaker doesn't display tables or equations in the color-style of the conditional text in which they are embedded. For example, this table:

TABLE 1 Example Table

A	Two
Horse	257.12
π	Eraserhead

is still covered by the Comment condition, even though it prints in black. You just have to assume that a table or an equation which is embedded in marked conditional text is also covered by that condition.

Finally, this is made even more confusing as one of the colors used in the diagrams is blur and one is magenta. The colors in the diagrams, though, are just colors; they are not intended to indicate membership in any kind of conditional text.

Sorry - this all makes it harder to review, but I can't do anything about it.

This version has been printed with both of these classes of text showing. If you prefer, I can send you a version with both of those classes hidden - as a customer would see it.

When you review it, I am particularly interested in

- whether I am revealing too much information on the main board to customers that haven't reached an agreement with us.
- whether I have deleted too much information on the demo board
- whether the wiring directions and code fragments for servo use are correct and complete.

I am also interested in whether or not I have, in my edits, screwed up some of the information that Bob Alkire, Stephen Uhler, Arshan Poursohi have given me.

This PDF has commenting enabled, so you should be able to make your comments and edits from within the PDF reader and they will survive when you save the PDF.

-Doug Shaker, dshaker@xs.com

Sun SPOT Development Kit

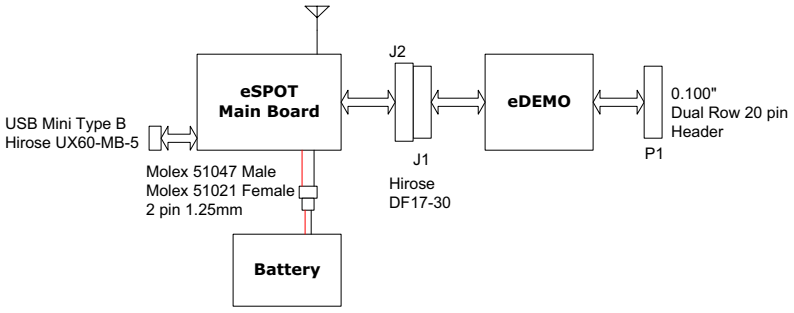
The current configuration of the Sun SPOT platform, the eSPOT, has a main processor running the Java VM “Squawk” and which serves as an IEEE 802.15.4 wireless network node. The eSPOT has flexible power management and can draw from rechargeable battery, USB host or be externally powered.

The Sun SPOT is designed to be a flexible development platform, capable of hosting widely differing application modules. The Sun SPOT development kit, as supplied, contains two different configurations. One of the configurations includes a demonstration application module, the eDemo board.

The configurations supplied in the kit are:

- Basestation - The basestation has an eSPOT main board without a battery or an application board. Power is supplied by a USB connection to a host workstation. The basestation serves as a radio gateway between other Sun SPOTs (and theoretically other 802.15.4 devices) and the host workstation.
- eSPOT - This unit contains the main board with a rechargeable LI-ION prismatic battery and an example of an eSPOT daughterboard, the eDEMO board.

FIGURE 1 eSPOT Board Configuration and Connectors:



The development kit also contains

- a wall-mount bracket for the eSPOT
- an eSPOT module adapter. This plastic replaces the top eSPOT plastic and allows the eSPOT to be attached to a larger circuit board.

Other plastics may be available from the Sun SPOT team in the near future.

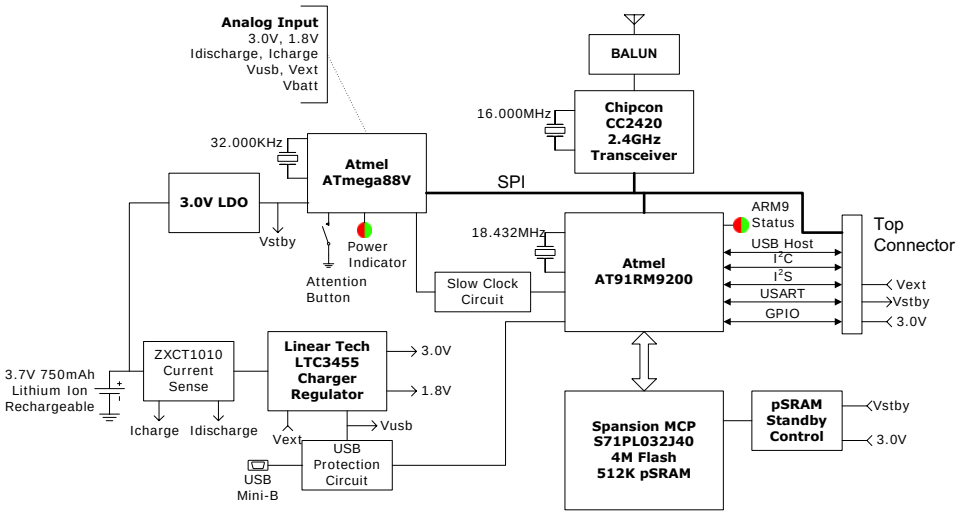
The eDEMO board is an example of the class of daughterboards that are compatible with the eSPOT main board. The eDemo board contains a 3-axis accelerometer, an ambient light sensor, eight tricolor LEDs, two push buttons, six analog input pads, four high current high voltage output pads, and five general I/O pads.

eSPOT Main Board

The eSPOT main board contains the

- main processor
- memory
- power management circuit
- 802.15.4 radio transceiver and antenna
- battery connector, and
- daughterboard connector

FIGURE 2 eSPOT Main Board Components



Main Processor

The main processor is an Atmel AT91RM9200 system on a chip (SOC) integrated circuit. This unit incorporates the ARM920T ARM Thumb processor, based on the v4T ARM architecture ARM9TDMI. The unit is packaged in a 256-pin ball grid array package measuring 15mm square and does not require a heat sink. Power to the SOC is 3.0V I/O voltage and 1.8V core voltage. In normal operation, it consumes approximately 44mW core power. The ARM executes at 180MHz maximum internal clock speed based on a software controllable phase lock loop/oscillator. The SOC contains a 64-way associative 16Kbyte data cache and a 16Kbyte instruction cache. The ARM9 uses a standard ARMv4 memory management unit with 64-entry instruction translation lookaside buffer (TLB) and 64-entry data TLB. The unit has standard IEEE 1149.1 JTAG boundary scan on all digital pins. These signals are brought to test pads on the bottom of the eSPOT board. This requires a production test fixture with pogo pin connector to access these pads. The JTAG signals are pulled up by 10K resistors to V_{cc}.

The external memory is controlled and accessed using the external bus interface (EBI) module. The EBI contains a static memory controller, SDRAM controller and burst flash controller. The eSPOT uses the static memory controller for interfacing to Flash and pSRAM memories. The SDRAM and burst flash controllers are not used and powered down. The static memory controller is configured to boot from Flash memory. The external memory databus is a 16-bit data path with byte-wide and word-wide access. It uses twenty-one address bits A1-A21 for word address with BS1 (UB) and BS0 (LB) byte and word address. CS_RAM (CS1) enables pSRAM access and CS_ROM (CS0) accesses FLASH memory. Memory is read when chip select and OE are asserted and written when chip select and WE are asserted.

The ARM9 is reset by the power controller as part of the power up and power down sequence. Reset also disables the pSRAM during power change to prevent accidental writes to memory.

The ARM920T has two clock sources that can be selected: BCLK and FCLK. The selected clock source will be used to generate its global clock, GCLK. FCLK is controlled from a software programmable phase lock loop (PLL). BCLK is controlled from the 32.768KHz real time clock oscillator and is enabled on startup. Initialization software then configures the phase lock loop and switches from BCLK to the faster FCLK.

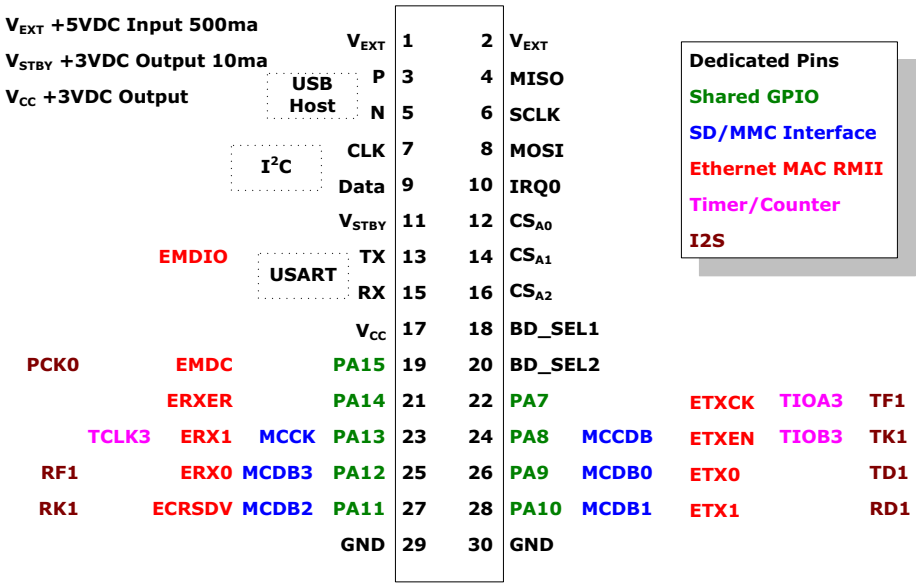
Rather than use a slow crystal with a 900msec start up time, we generate an instant 32.7KHz square wave from the power controller. We run the square wave through an attenuator and a three-pole elliptic-caure low-pass filter to create a 120mV 32.7KHz sine wave to the real time clock oscillator. This clock starts when V_{ddio} reaches 1.5V and shuts off when the ARM is placed into deep-sleep.

The SOC has a large collection of peripheral interface units. These include USB host port, USB device port, Ethernet MAC, programmable I/O (PIO) controller, serial peripheral interface (SPI) controller, TWI two-wire (I2C) interface, universal

synchronous/asynchronous serial interface (USART), serial synchronous controller (I2S), multimedia card interface, three 16-bit counter/timers and system timers. The unit also contains a real-time clock which is unused. The SOC also contains a peripheral DMA controller (PDC) for fast direct access to USART, I2S, SPI and memory channel.

The USB host port, one USART, and the multimedia card, TWI, I2S and Ethernet MAC interfaces are not used directly in the current eSPOT implementation although all signals are brought to the interboard connector. These peripherals could be used provided the appropriate physical interface and driver software. As this is a small unit, not all devices can be utilized simultaneously. Please see pin out description of the interboard connector, FIGURE 3, for more information.

FIGURE 3 Interboard Connector



Main Board Communication

USB

The USB client has termination and ESD protection circuit U9 to a type B mini USB connector. The USB device is USB 1.1 and USB 2.0 compliant. A 1.5K resistor pulled to 3.3V from V_{usb} is switched on by FET Q3 when USB_PUP is asserted. The 1.5K resistor is on the D+ signal indicating full speed device during start-up. The USB

client supports CDC Abstract Control Mode (ACM) modem interface for serial communication. Currently no other endpoints are supported. Basestation SPOTs interact with the host workstation principally through the USB client.

SPI

The SPI interface is the primary interface to most on-board devices and for interboard communications. Within the eSPOT main board, SPI is the communication channel to the radio transceiver IC CC2420 and the power controller.

SPI communication relies on four signals:

- MOSI (Master Out, Slave In)
- MISO (Master In, Slave Out)
- SCLK (Synchronous Clock)
- CS (Control Strobe)

The ARM9 is master in all conditions. PIO signals provide the active low control strobes (CS). MISO and MOSI are the tri-stateable serial data lines and the SCLK is the synchronized clock for the data originating from the master.

SPI shifts out bytes most significant bit first, synchronized either to the rising or falling edge of SCLK. While it is shifting out on MOSI, it is shifting in to a holding register from MISO. Chip select is asserted prior to shifting and deselected after a byte transfer. Each slave device has a unique chip select and removes tristate from MISO only when the slave is selected.

The CS for the power controller is AVR_CS (PA6/PCS3). The CS for the CC2420 radio transceiver is RF_CS (PA5/PCS2). Interboard chip select uses a primary "board" select of BD_SEL1 (PA3/PCS0) and BD_SEL2 (PA4/PCS1). A secondary three bit address allows selection of eight devices for each board select. The secondary address, from least significant bit to most is CS_A0 (PB15), CS_A1 (PB16) and CS_A2 (PB17). The secondary address lines must be selected and stable prior to BD_SELx asserted and must remain stable until after BD_SELx is deasserted. For stacking boards, BD_SEL1 will select the board nearest the main board, and BD_SEL2 will select the stacking board. BD_SEL1 is used when only one application board is present.

Every application board is required to have a small SPI EEPROM selectable when CS_A0 = '1', CS_A1 = '1' and CS_A2 = '1'. This memory is for board identification and configuration information.

Programmable Input/Output (PIO)

The bicolor LED closest to the center of the unit is controlled by the PIO interface. The red LED2 uses PIO PB24 and green LED1 uses PIO PB23. USB power control signals USB_PUP output from PIO PA21 controls USB pull-up enable, USB_PWR_MON is high when USB power available and input to PIO PA22, USB_EN is output from PIO PA20 and controls the suspend line on the power regulator, USB_HP is output from PIO PA19 which sets power control into high power mode when high.

PIO bits also control signals or read status to and from the radio transceiver. The signals are:

- FIFOP input to PIO PA23 indicates RX fifo full
- FIFO input to PIO PB2 indicates bytes are in the receive buffer,
- RF_PDOWN (VREG_EN) output from PIO PB1 turns the local regulator on,
- SFD input to PIO PB4 indicates start of frame,
- CCA input to PIO PB3 indicates clear channel assessment
- RF_RST output from PIO PB0 forces the transceiver to reset when asserted low.

For more information on ARM920T technical specification and the AT91RM9200 datasheet from the Atmel website.

Memory

Memory is a single Spansion S71PL032J40, a multichip package (MCP) consisting of a 4MByte NOR Flash memory and a 512KByte pseudo-static random access memory (pSRAM). The Flash memory and pSRAM die are stacked on a single 56-pin fine pitch ball grid array, 9mm x 7mm. The access time of the pSRAM is 70nsec and the flash memory is 65nsec. The pSRAM is self-refreshing and automatically enters power down when not selected for access. Memory contents are maintained as long as a power supply USB, external or battery is connected - even during periods of off or "deep-sleep".

Flash and pSRAM are both 16-bit data paths and are byte and word accessible. There are 21 address lines, upper and lower byte strobes, output enable, write enable, pSRAM chip selects and flash chip select. The BUSY signal from the MCP can indicate refresh in progress, write to flash in progress to hold off the processor. BUSY goes to PIO PC14 on the processor. The write protect (WP) is disabled by a pullup to V_{cc}.

The unit is powered from a single 3.0V supply with individual and separate power pins for Flash and pSRAM. Power to the pSRAM is controlled by a FET switch U10, Analog Devices ADG819. This switch is controlled by the power controller. When the unit is in deep sleep, it switches to a very low current standby voltage which

maintains the memory contents. When the power controller powers the processor, the switch is set to use the higher current V_{cc} source. Power consumption of the pSRAM during deep-sleep is approximately 8µA. Power is removed from flash during deep-sleep. During normal operation, pSRAM consumes 25ma and Flash consumes 22ma.

Flash memory uses a common flash interface with erase, sector write and random and page mode read operations. The Flash memory is divided into 4Kword (boot, both top and bottom) and 32Kword sectors with one million write sector cycles.

Flash is preprogrammed with the bootloader, VM, base class libraries and applications at the factory. The customer lockable area (0x000040-0x00007f) is programmed at the factory with a 64-bit IEEE extended unique identifier (EUI). The IEEE EUI is read only and is a concatenation of a 24-bit company code (OUI) and with a 40-bit extension that is unique for each SPOT.

Power Circuit

The eSPOT can be powered with any combination of rechargeable battery, external voltage or the USB Host. The power circuit charges the battery, regulates the power to the main and application boards, provides standby power during deep-sleep, maintains a 64-bit millisecond clock with alarm, monitors power levels and manages the attention button and power LEDs.

The power regulation portion of the circuit is the Linear Technology LTC3455 U2. The LTC3455 is an integrated Li-ION battery charger, USB power manager and dual switching regulator. The current mode step-down switchers run at 1.5MHz and output 3.0V at 500ma (V_{cc}) and 1.8V at 200ma (V_{core}). The V_{cc} switcher is similar to the LTC3406 and the V_{core} switcher is similar to the LTC3405. The Li-ION battery charger is constant current charger similar to the LTC4053. The switching regulators (not the charger) are turned on by the PWRON signal from the power microcontroller. The LTC3455 is packaged in a 24-pin QFN (Quad Flat package no leads) 4mm square.

The LTC3455 current limits the USB current to 100ma when USB_HP is low and 500ma when USB_HP signal is high. USB_HP is controlled by the ARM9 PIO PA19. External voltage is not affected by USB_HP; however, 100ma incoming current only allows the ARM9 to run in order to negotiate for more power. If the SPOT is running without a battery, powered only by the USB, the application board and radio should be powered down until the device is fully enumerated and can set the higher current. The ARM9 can shut down the USB regulator and battery charger with the USB_EN signal. USB voltage and external voltage have a “snubbing” RC filter to protect against insertion voltage surges.

When either external or USB power is applied and the battery is below 4.05V, a timed constant current charge will start. This should last approximately three hours and the maximum charge current is 450ma. If the battery below 3.0V, the regulators will not start. If the die reaches 105ºC, charge current is greatly reduced.

A very low quiescent current LDO voltage regulator, TI TPS79730 U6, generates 3.0V for standby voltage needs. The LDO power input is from any of the power sources and provides constant uninterruptable power to the Atmega88 microcontroller, the pSRAM portion of the MCP memory and the pullup on the attention button. The LDO also generates a brown-out detect which pulls the reset low on the Atmega88 should the voltage drop below the Atmega88 operating parameters. If the battery is not present and power is discontinued or if the battery voltage falls below 3.0V, the real time clock or alarm will not function.

Deep Sleep, Idle and Run Modes

John Daniels submitted a diagram and a rewrite of original version of this section. I have attempted to merge this with the initial information supplied by Bob Alkire while maintaining a hardware (rather than a software) focus. Please take a look.

Sun SPOTs have power conservation firmware that uses three modes of operation:

Run Basic operation with all processors and radio running. Power draw for the eSPOT board in Run mode is between 70ma and 120ma. The application daughter board can consume up to 400ma if enabled.

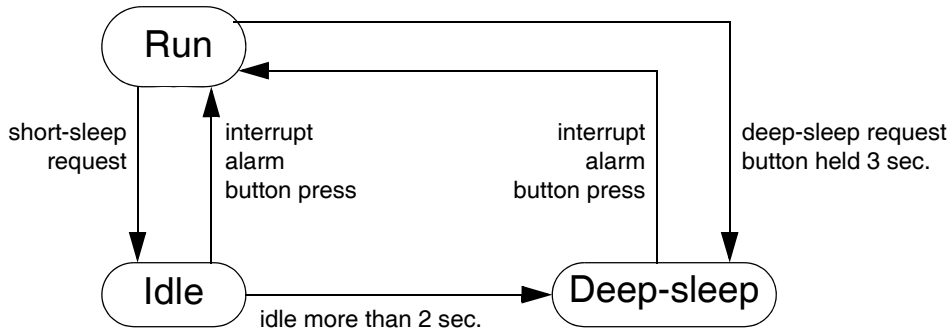
Idle ARM9 clocks are shut off and the radio is off. Idle mode power consumption is about 24ma.

Deep-sleep All regulators are shut down except for the standby LDO, the power-control Atmega and pSRAM. Deep-sleep power consumption is 32µA. Typical start-up time from deep-sleep is about 2msec to 10msec.

Deep-sleep can not be entered if the radio is on, if external power is supplied, or if USB power is on.

Deep-sleep and idle are entered programmatically. Deep-sleep can also be entered by holding the attention button more than 3 seconds. Waking the processor up from deep-sleep can be done with the alarm, an external interrupt or pressing the attention button.

FIGURE 4 Power Consumption Mode Transitions.



The sequence of events for start up when it is initiated is first the external interrupt is disabled, the ARM9 is held in reset, the internal power monitor ADC begins and then PWRON to the power regulator is asserted. The ADC tracks the V_{cc} and V_{core} voltages as the regulators reach full voltage. When V_{cc} reaches 1.1V, the internal timer used to generate the 32.7KHz start up clock to the ARM9 starts oscillating. When V_{cc} has reached a stable 3.0V, the pSRAM voltage is switched from standby LDO to V_{cc} and the ARM9 is brought out of reset. Status bits are available to the ARM9 to indicate how the startup was initiated to determine continuing from a known context or restarting.

Battery

The internal battery is a 3.7V 720maH rechargeable lithium-ion prismatic cell. The battery has internal protection circuit to guard against over discharge, under voltage and overcharge conditions. The battery can be charged from either the USB type mini-B device connector or from an external source with a 5V ±10% supply. Typical shelf life losses at room temperature are about 2% of the batteries capacity per month and the rate can increase with the rise in temperature.

The battery can ***not*** be changed for another type of battery. The charging and power management systems are tuned for this specific battery. The risks associated with battery substitution are substantial.

The simplest, safest, and easiest way of extending the operating period of a Sun SPOT beyond the length of one battery charge is to provide USB power. There are a variety of USB power dongles available on the market, including AC and battery-powered models.

Battery Warnings

Do not short-circuit battery. A short-circuit may cause fire, explosion, and/or severe damage to the battery.

Do not drop, hit or otherwise abuse the battery as this may result in the exposure of the cell contents, which are corrosive.

Do not expose the battery to moisture or rain. Keep battery away from fire or other sources of extreme heat. Do not incinerate.

Exposure of battery to extreme heat may result in an explosion.

No other battery substitutions or different chemistry batteries should be used.

Do not bypass the battery protection circuit.

Dispose of batteries properly. Do NOT throw these batteries in the trash. Recycle your batteries, if possible.

Power Controller

The power controller is an 8-bit microcontroller Atmel Atmega88. Its firmware is responsible for keeping a 64-bit millisecond real time clock running, waking up the system when an alarm occurs, waking up the system if an external interrupt is seen from the application module, and waking up and putting the system into deep-sleep from the attention button. The power controller also measures the battery voltage, the battery charge current and discharge current, V_{cc} voltage, V_{core} voltage, V_{ext} external voltage, and USB voltage V_{usb}. The Atmega88 also controls a bicolor LED (Power LED) and indicates various modes and fault conditions through this LED. The Atmega88 has a low frequency 32.000KHz crystal prescaled by 32 for an increment per millisecond of one of the internal timer/counters.

The Atmega88 interacts with the ARM9 through the SPI channel as a slave device and using AVR_CS (PCS3) as the enable. The first byte sent is the command and subsequent bytes transfer status and parameters to and from the Atmega88. The power controller can interrupt the ARM9

While in run or idle mode, the built-in 10-bit A/D converter measures all of the seven voltage/current levels every 50ms. It uses a 1.1V internal reference for measuring battery voltage and the 3.0V standby regulator as an external reference for all other measurements.

The battery current is measured by monitoring the voltage drop across a 0.1Ω resistor using high-side current sensors Zetex ZXCT1009 U4 for discharge and U3 for charge. Current measurement resolution is 0.5ma and can measure a maximum of 512ma to or from the battery. The battery voltage is enabled by a FET switch Q1 and Q2 and divided by series resistance. The microcontroller enables this switch only when reading the battery voltage and disables it all other times to minimize current drain.

Equations for calculating value to units are as follows:

TABLE 2 ADC Equations

Signal	Equation
V_{batt}	$ADC = \frac{V_{batt} \cdot 1024}{5.1}$ *volts*
V_{cc}	$ADC = \frac{V_{cc} \cdot 1024}{3.904}$ *volts*
V_{core}	$ADC = \frac{V_{core} \cdot 1024}{3.0}$ *volts*
V_{ext}	$ADC = \frac{V_{ext} \cdot 1024}{6}$ *volts*
V_{usb}	$ADC = \frac{V_{usb} \cdot 1024}{6}$ *volts*
I_{charge}	$ADC = I_{charge} \cdot 2$ *milliamps*
$I_{discharge}$	$ADC = I_{discharge} \cdot 2$ *milliamps*

After each measurement, the values are compared to acceptable ranges of values. If any of these values go outside, the power light indicates a power fault. If the battery is approaching fully discharged state, it will show a low battery indication. If the unit is charging, it will show a charge indication.

TABLE 3 Voltage Ranges

Voltage	Target	Error states
V_{cc}	3.0V ±10%	2.7V or > 3.3V power fault
V_{core}	1.8V ±10%	< 1.62V or > 1.98V power fault
V_{usb}	5.0V ±10%	< 4.5V or > 5.5V power fault
V_{ext}	5.0V ±10%	< 4.5V or > 5.5V power fault
$I_{discharge}$	< 500ma	> 500ma power fault
V_{batt}	> 3.25V	< 3.25V indicates low battery
V_{batt}	> 3.05V	< 3.05V indicates dead battery
I_{charge}	< 5ma	> 5ma indicates charging

Wireless Radio

The wireless network communications uses an integrated radio transceiver, the TI CC2420 (formerly ChipCon). The CC2420 is IEEE 802.15.4 compliant and operates in the 2.4GHz to 2.4835GHz ISM unlicensed bands. Regulations for these bands are covered by FCC CFR47 part 15 (USA), ETSI EN 300 328 and EN 300 440 class 2 device (Europe) and ARIB STD-T66 (Japan). Please check with country statutes for appropriate operation.

The IC contains a 2.4GHz RF transmitter/receiver with digital direct sequence spread spectrum (DSSS) baseband modem with MAC support. Other features include separate TX and RX 128 byte FIFOs, AES encryption (currently not supported), received signal strength indication (RSSI) with 100dB sensitivity and transmit output power setting from -24dBm to 0dBm. Effective bit rate is 250kbps and chip rate is 2000kChips/s. Receive sensitivity is -90dBm.

The digital control and data communications with the CC2420 use PIO port bits and the SPI channel. The CC2420 is a slave SPI bidirectional device addressed when RF_CS (PCS2) is asserted active low. PIO ports reset the CC2420 (RF_RST), power it down (RF_PWDOWN), or check the status of the receive FIFO (FIFO and FIFOP), clear channel assessment (CCA) and start of frame (SFD).

There are 33 configuration and status registers, 15 command registers and two 8-bit registers for the separate transmit and receive FIFOs. The first byte sent to the CC2420 is the address made up of 6-bit address, RAM/Register select (Bit 7) and Read/Write select (Bit 6). Following bytes are data read from or written to the CC2420.

The CC2420 is housed in a 48pin quad leadless package (QLP or QFN) that is 7mm square. It is powered with +3.0V Vcc supply. The CC2420 has an internal 1.8V low drop out regulator for powering the internal RF and analog circuitry. It consumes 20ma during receive operation and 18ma for 0dBm transmit. The frequency generation uses an accurate 16MHz crystal with ±10ppm accuracy, ±10ppm stability and ±1ppm aging. The entire RF section is enclosed in an upper and lower RF shield and has modular FCC approval.

TABLE 4 802.15.4 Channel Assignment

Channel	Center Frequency	Channel	Center Frequency
11	2405MHz	19	2445MHz
12	2410MHz	20	2450MHz
13	2415MHz	21	2455MHz
14	2420MHz	22	2460MHz
15	2425MHz	23	2465MHz
16	2430MHz	24	2470MHz
17	2435MHz	25	2475MHz
18	2440MHz	26	2480MHz

The output power can be adjusted by the PA_LEVEL register, a 6 bit field.

TABLE 5 PA_Level and Output Power

PA_LEVEL	Output Power	PA_LEVEL	Output Power
31	0dBm	15	-7dBm
27	-1dBm	11	-10dBm
23	-3dBm	7	-15dBm
19	-5dBm	3	-25dBm

For more information, see the CC2420 data sheet on the www.ti.com (RF/IF Components) or www.chipcon.com. The 802.15.4 standard can be retrieved from standards.ieee.org.

Antenna

The antenna is an inverted-F antenna printed on the top layer of the printed circuit board. It is tuned to 2450MHz and has a characteristic input impedance of 115Ω unbalanced. This is a folded monopole λ/4 wave with reasonable omnidirectional radiation. The antenna is matched to the balanced RF output of the CC2420 using a lumped-LC network. The RF output is also biased by the TXRX_SWITCH output of the CC2420 through a RF blocking filter.

The antenna section of the eSPOT should be kept away from all metal objects. If mounted on a motherboard, there should be no pcb traces or power planes under or around the antenna section. If possible, the eSPOT should be mounted so that the antenna is located on the edge of the board.

The FCC certification does not allow an external antenna to be connected to the eSPOT.

eSPOT Daughterboards

The supplied eDemo board is a single example of the class of daughterboards which may be connected to the eSPOT main board. Any eSPOT daughterboard must have at least the following characteristics:

- connect to the eSPOT main board with a Hirose DF17-30 connector
- act as an SPI slave in communication with the eSPOT main board
- contain SPI flash memory for storing configuration information

Communication from the main board to any daughterboard is done through the SPI channel. The main board select is BD_SEL1. This is an addressable control signal which uses signals CS_A0 - CS_A2 as the address lines of a 3-to-8 decoder (74LVC138). The chip selects are enabled when BD_SEL1 is asserted active low.

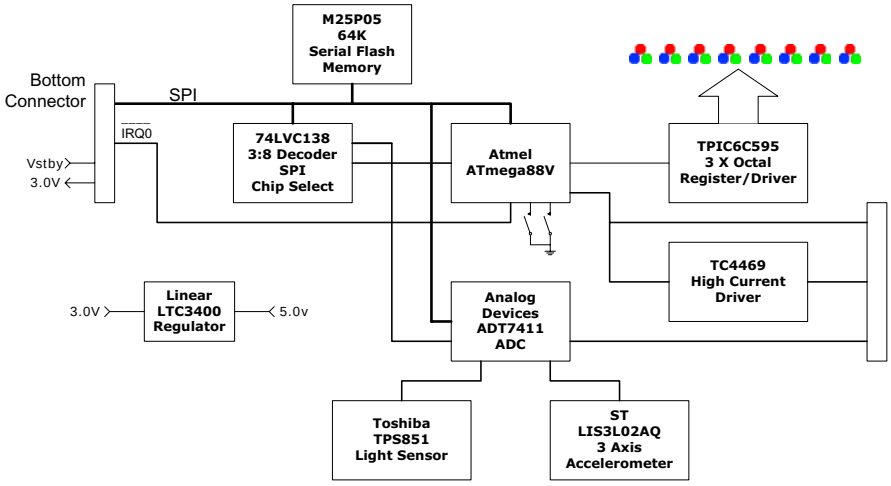
The three-bit chip select address allows eight devices for each board select. CS_A2, CS_A1 and CS_A0 must be selected and stable prior to BD_SELx asserted and remain stable until after BD_SELx is deasserted. For stacking boards, BD_SEL1 will select the board nearest the main board, and BD_SEL2 will select the stacking board. BD_SEL1 is used when only one application board is present.

Every application board is required to have a small SPI flash selectable when CS_A0 = '1', CS_A1 = '1' and CS_A2 = '1'. This memory is for board identification and configuration information.

eDemo Board Hardware

The supplied eDemo board is an example from the possible universe of eSPOT daughterboards. It contains an Atmega88 processor, flash memory, a light sensor, an accelerometer, eight tri-color LEDs and two switches.

FIGURE 5 eDemo Board Components



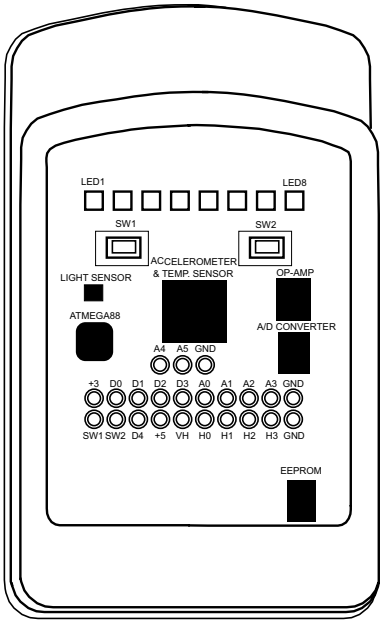
The Atmel Atmega88 microcontroller communicates with the main board ARM9 over the SPI channel as a slave device. The Atmega88 controls the LEDs, provides general multifunction input/output pins, interrupts the ARM9, controls mode bits on the accelerometer, scans analog inputs and reports digitized values. New firmware for the eDEMO board can be loaded over the SPI channel.

The chip select address truth table is

TABLE 6 Chip Select Address Truth Table

BD_SEL1	CS_A2	CS_A1	CS_A0	Function
1	X	X	X	No Operation
0	1	1	1	Select configuration memory
0	1	1	0	Reserved
0	1	0	1	Reserved
0	1	0	0	Reserved
0	0	1	1	Reserved
0	0	1	0	Select ATD7411 ADC (ADC_CS)
0	0	0	1	Select Atmega88 RESET (Program mode)
0	0	0	0	Select Atmega88

FIGURE 6 eDemo Board Component Locations



I/O Connector Pinout *P1*

V_{CC} +3VDC Output 100ma Maximum	**SW1**	**1**	**2**	**V_{CC}**
V_{+5V} +5VDC Output 100ma	**SW2**	**3**	**4**	**D0**
V_H +4.5V to 18VDC Input	**D4**	**5**	**6**	**D1**
A0-3 Analog Input 10 bit 0V to 3.0VDC	**V_{+5V}**	**7**	**8**	**D2**
D0-4 GPIO	**V_H**	**9**	**10**	**D3**
H0-3 High Current Output 125ma 0V to V_H	**H0**	**11**	**12**	**A0**
	H1	**13**	**14**	**A1**
	H2	**15**	**16**	**A2**
	H3	**17**	**18**	**A3**
	GND	**19**	**20**	**GND**

The I/O connector is designed for a 20-pin through-hole 0.1" center header. V_{cc} comes from the eSPOT. V_{+5} is generated on the eDEMO board.

Configuration Memory

All application boards have a serial EEPROM memory for storing configuration information. On the eDEMO board this is an SPI EEPROM 64K x 8 U8 which is enabled when CS_A2-CS_A0 = '111'. This memory can be written to and read from.

LEDs

Along the top of the eDEMO board is a row of eight tricolor (red-green-blue) LEDs LED1-LED8. These LEDs are driven by octal driver/registers STPIC6C595 U9-U11. The driver/registers are serially loaded by the on-board Atmega88. The synchronous serial stream to the LEDs is RED0-RED7, GREEN0-GREEN7 and BLUE0-BLUE7. After the 24bits are shifted in, the LED_EN broadside loads the shifted bits to the LEDs. This register is reloaded every 255µs and the bits are pulse-width modulated in firmware to vary the individual intensity of each LED. The LED intensities are set by SPI commands from the ARM9.

Pushbuttons

Below the LEDs are two tactile momentary SPST normally open pushbuttons, SW1 and SW2. These are scanned by the Atmega88 processor and can report the state of the pushbutton to the ARM9 over SPI. The pushbuttons are pulled up to +3V, either V_{cc} or V_{stby} and are high to AVR port pins PB0 and PB1. Pushing a button will pull the signal on PB0 or PB1 to ground. The pushbuttons signals go to connector P1 pin

1 (SW1) and P1 pin 3 (SW2) through 1K ohm resistors. These pins can either be input to the eDEMO board and parallel the operation of the pushbuttons, or they can passively monitor the pushbuttons as outputs.

GPIO

The general purpose digital I/O lines may be configured as either inputs or outputs. D0 and D1 may also be used as UART data lines RX and TX. D2 and D3 may also be used as I2C-DATA and I2C-CLOCK respectively.

The current limitations on the GPIO lines depend on the temperature of the Sun SPOT. At room temperature, the limits are source current, 16ma; sink current, 24ma. For other temperatures, see the Atmega88 datasheet, assuming 3.0v to the Atmega88.

High current Driver

Four signals from the Atmega88 PC0-PC3 are buffered by a high current driver, Microchip TC4469. The outputs, H0-H3, are totem-poll capable of sinking and sourcing 125ma. The high voltage output is set by V_H which is externally connected to P1 pin 9. V_H is between +4.5V to +18VDC and must be connected to a positive supply for H0-H3 to function.

Analog to Digital Conversion

The Analog Devices ADT7411 ADC is used to convert analog inputs from the accelerometer and light sensor to digital outputs for the Atmega88. The ADC is also available to encode analog inputs from pins A0, A1, A2, and A3.

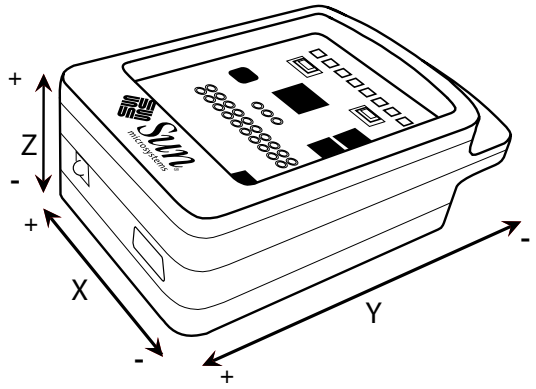
The analog inputs are designed to accept a 0 - $3V_{dc}$ analog voltage.

The resolution is 1.024mV/count. $ADC = \frac{V_{in} \cdot 1024}{V_{ref}}$. V_{ref} is 3.0V.

Accelerometer

The eDEMO board contains the ST Microsystems 3-Axis 2g/6g Inertial Sensor LIS3L02AQ. The Z axis is perpendicular to the boards surface, the Y axis is parallel with the boards surface perpendicular with the row of LEDs, and the X axis is parallel with the row of LEDs.

FIGURE 7 Orientation of X, Y, and Z Accelerometer Axes.



The accelerometer has three voltage outputs V_{out_x}, V_{out_y} and V_{out_z} representing acceleration in 3-axis. The force accerating the SPOT in any dimension, measured in g-force units, is:

$$g = \frac{ADC - 465.5}{186.2}$$

These are filtered by a single pole filter (0.01µF capacitor) and buffered by non-inverting op amp U3. The output of the op-amp is voltage divided by a 10/11 ratio with a 1.0K and 10.0K 1% resistors and is the input to channels 6(x), 7(y) and 8(z) of the ADC U4 (ADT7411). Taking the ratio into account,

$$ADC = \frac{V_{in} \cdot (10/11) \cdot 1024}{V_{ref}} = \frac{V_{in} \cdot 931}{V_{ref}}$$

The accelerometer output reference is 0g = $V_{dd}/2$ = 1.5V with 2g sensitivity of ($V_{DD}/5$)V/g or 600mV/g ±10%, 6g sensitivity of ($V_{DD}/15$)V/g or 200mV/g and a range of 0.3 to 2.7V. At the ADC the range is 272mV to 2.455V and 0g at 1.364V. Sensitivity is 545mV/g at the ADC for 2g and 182mV/g for 6g. Nominal 0g read from the ADC is 466.

$$V_{acc} = (600mV \cdot g) + 1500mV$$

$$ADC = \frac{\left(((600mV \cdot g) + 1500mV) \cdot \left(\frac{10}{11}\right) \cdot 1024\right)}{V_{ref}}$$

$$ADC = 186.2g + 465.5 \qquad for \qquad V_{ref} = 3.0V$$

$$g = \frac{(ADC - 465.5)}{186.2}$$

For each axis, the maximum sample rate is 160hz. The capacitors C5-C7 provide a single pole low pass filter to bandlimit the accelerometer. The frequency of this limit is

$$F_t = \frac{1}{2\pi \cdot R_{out} \cdot Cf(x, y, z)}$$

C5-C7 are 0.01µF capacitors and R_{out} is 100K internal resistance of the accelerometer. Therefore the cutoff frequency F_t is 160Hz.

Accelerometer Self Test

The accelerometer has a self test mode which physically biases the internal "slug" with electrostatic energy. Self test is the measured difference between normal mode and self-test mode. Self-Test mode is entered when the self-test pin is set to a '1'. During these test, the accelerometer must be stationary. Two readings are taken of all three axis. The first reading is in normal mode, the second is in 'self-test' mode. The difference between normal and self-test mode for each axis must fall within a specified range (see TABLE 7). This test is performed in both 2g and 6g settings.

TABLE 7 Range for Normal to Self-Test

Mode	Axis	Voltage Range	Reading
2g	X_axis	-20mV to -40mV	-6 to -13
6g	X_axis	-6mV to -14mV	-1 to -5
2g	Y_axis	20mV to 40mV	6 to 13
6g	Y_axis	6mV to 14mV	1 to 5
2g	Z_axis	20mV to 50mV	6 to 16
6g	Z_axis	6mV to 17mV	1 to 6

Light Sensor

Light sensor is mounted on top of the eDEMO board using a Toshiba TPS851 light to voltage sensor. The output of the sensor is 0.1V to 4.3V, dark to light, using a emitter resistor of 4.7K (R4). This voltage is buffered by op-amp U3 (TI TLV2434) and divided by 2 by resistor divider R5 and R9. The output of the resistor divider is input to channel 5 of the ADC U4 (ADT7411) with an effective range of 0.05V to 2.15V.

Peak sensitivity of light sensor is 600nm. >3dB sensitive is ±45° and switching time is ~30µsec.

TABLE 8 Specified Typical Values for Light in Luminance (lx) Versus Voltage

Luminance	Light Sensor Voltage	ADC Voltage	Raw ADC
1000 lx	2.914V	1.457V	497
100 lx	0.291V	0.146V	50
10 lx	0.029V	0.014V	5

$Lux \approx 2 \cdot ADC$

Electrical Characteristics

TABLE 9 Absolute Maximum Ratings

Operating Temperature (with battery charging)	0 to 45C
Operating Temperature (with battery discharging)	-20 to 60C
Operating Temperature (without battery)	-20°C to +75°C
Storage Temperature (with battery)	-20°C to +35°C
Storage Temperature (without battery)	-40°C to +85°C
Voltage on any input pin	-0.1V to 3.5V
eDEMO DC Current per I/O pin	40.0ma
eSPOT DC Current per I/O pin	8.0ma
Maximum External/USB voltage	6.0V

TABLE 10 DC Characteristics - eSPOT J2 Connector

Symbol	Description	Condition	Min	Typ	Max	Units
V_{ext}	External Voltage		4.2	5.0	5.5	V
V_{batt}	Battery Voltage		3.1	3.7	4.2	V
V_{usb}	USB Voltage		4.2	5.0	5.5	V
I_{usb}	USB Current Limit	V_{usb} = 5.0V, USBHP = '1' V_{usb} = 5.0V, USBHP = '0	440 60	475 80	500 100	ma ma
I_{ext}	External Current	V_{ext} = 5.0V, no eDemo V_{ext} = 5.0V, with eDemo		300 500		ma ma
I_{batt}	Battery current - no attached board	Deep Sleep Idle Normal	18 21 40	21 23 87	28 25 144	µa ma ma
I_{charge}	Charge Current	V_{usb} = 5.0V, USBHP = '1' V_{usb} = 5.0V, USBHP = '0' V_{ext} = 5.0V	 425	400 50 500	470 90 575	ma ma ma
V_{low_batt}	Low battery indication			3.25		V
I_{stby_max}	Externally available standby current	J2-11 V_{stby} = 3.0V			5	ma
I_{CC}	Attached board current	V_{CC} = 3.0V				ma
V_{OL}	Output low level voltage	I_{OL}= 0 to 8ma	0.2	0.3	0.4	V
V_{OH}	Output high level voltage	I_{OH}= 0 to 8ma	2.6	2.7	2.8	V
V_{IL}	Input low level voltage		-0.3		0.8	V
V_{IH}	Input high level voltage		2.0		2.7	V

TABLE 11 DC Characteristics - eDEMO I/O Connector *P1*

Symbol	Description	Condition	Min	Typ	Max	Units
V_{ext}	External Voltage		4.2	5.0	5.5	V
I_{ext}	External Current	V_{ext} = 5.0V				ma
I_{CC}	eDEMO current from main board.	V_{CC}=3.0V			250	ma
V_{+5V}	5V output from eDEMO at P1-7	V_{+5V}=+5.0V			100	ma
V_H	H0-H3 high level voltage		4.5		18	V
V_{OL}	Output low level voltage (except for H0-H3)	I_{OL}= 6ma	--	--	0.5	V
V_{OH}	Output high level voltage (except for H0-H3)	I_{OH}= 10ma	2.3	--	--	V
V_{OL}	Output low level voltage for H0-H3	I_{OL}= 0 to 8ma	--	--	0.15	V
V_{OH}	Output high level voltage for H0-H3	I_{OH}= 0 to 8ma	V_H-0.025	--	--	V
I_H	H0-H3 output current sink/ source	Single Output All Outputs			300 500	ma ma
V_{IL}	Input low level voltage	All inputs	-0.5	--	0.9	V
V_{IH}	Input high level voltage		1.8	--	2.5	V
V_{ANA}	Input voltage range		0.0		3.0	V

eDemo Software

The eDemo board contains an Atmega88 micro-controller. This section describes the functions implemented in the Atmega88 firmware.

Overall operation

The Atmega88 operates the 8 tricolor LEDs, the accelerometer configuration, and the following pins on the I/O header:

```
D0, D1, D2, D3, D4,
H0, H1, H2, H3, SW1, SW2,
ADC4, ADC5, GND.
```

The Atmega88 communicates with the main board using an SPI interface. The Atmega88 also controls an interrupt line to the power controller on the main board.

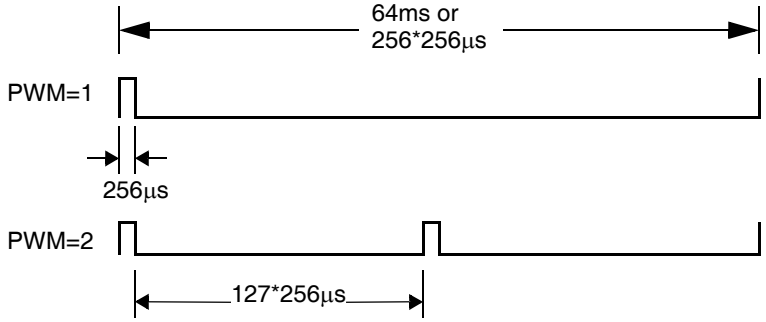
The Atmega88 operates with an 8mhz instruction clock. Every 256µs, the controller runs its process loop to execute the tasks currently enabled. When all the tasks are completed, the processor goes to sleep until the next process interrupt.

Functions

Pulse Width Modulation

This function supports pulse width modulation (PWM) on up to 8 I/O pins simultaneously. For any particular pin, PWM value may be set to any integer between one and 255. The output state will be high for that number of evenly spaced

periods of 256µs out of a 64ms cycle. If the value is one, the output will be high for



256µs and low for (255*256)µs. When the value is two, the output will be high for 256µs, low for (127*256)µs, high for 256µs, and low for (127*256)µs. When the value is 128, the output will be toggled between 1 and 0 every 256µs.

LEDs

Each of the 8 tri-color LEDs can be pulse width modulated using the PWM mechanism described above. Each of the red, green, and blue LEDs is separately controllable. The minimum value is limited to 3 to mitigate visible flicker.

If the Atmega88 processor is unable to complete all the tasks enabled in its process loop, it will suspend PWM of the LEDs temporarily.

Pulse Width Generation

A one-shot pulse can be generated on any output pin, with a pulse width ranging from 1µs to 65536µs. The pulse may be either positive (0 -> 1 -> 0) or negative (1 -> 0 -> 1). Only one pulse may be active at a time.

Pulse Width Detection

The duration of a pulse may be measured on any input pin, with the pulse width range from 1µs to 65536µs. Pulses longer than 65536µs will be recorded as 65536µs. As with pulse width generation above, the pulse may be either positive or negative. Only one pulse measurement may be active at one time.

Tone Generation

A square wave may be generated on any output pin. The frequency of the square wave will determined by the equation:

$$freq = \frac{500000}{N}$$

where *N* is the number input to the tone generator.

The period of the square wave is from 1 to 65536 units, where 1 unit is 2µs. To minimize the CPU load on the micro-controller, the current implementation has a minimum period of 129 units. Only one tone generator may be active at one time.

Servo Controller

Eight output pins may be configured to drive standard servos. For each servo configured output pin, a pulse is generated every 32ms. The pulse width generator (described above) is used to generate the pulses, and is not available separately when the servo controller is active. The pulse width is specified in µs and a typical value will be between 1000µs and 2000µs.

Servo would ordinarily be connected to a Sun SPOT by

- connecting the ground wire from the servo connector to the ground pin on the IO header
- connecting the data wire to one of the data input/output pins (D0 to D3) or the high output pins (H0 to H3)
- connecting the servo to a external power source

The following code fragment illustrates the steps to initiate a servo attached to pin D1 and set a pulse width for that servo.

```
import com.sun.spot.sensorboard.EDemoBoard;
import com.sun.spot.sensorboard.capabilities.IServoController;
import com.sun.spot.sensorboard.io.IOutputPin;
import com.sun.spot.sensorboard.peripheral.IServo;

// Get the demo board itself
EDemoBoard ourDemoBoard = EDemoBoard.getInstance();
// Create an object to hold the particular pin of interest
// on the demo board
IOutputPin servoOutPin = ourDemoBoard.bindOutputPin(
                 ourDemoBoard.getInstance.().D1);
// Bind a servo to that output pin
IServo ourServo = ourDemoBoard.bindServo(servoOutPin);
// Set the output pulse length to use for that servo
ourServo.setValue(1300);
// Also declare a relative position for that output pulse length
```

```
ourServo.setPosition(0.5);
// Now we can manipulate the servo by setting the pulse width or by
setting the position as a floating point number between 0 and 1.
```

Analog/Digital Conversion

The pins A0 to A3 are connected to the A/D converter (ADC) on the eDemo board. These can be read in sofware. If ADC is the digital output value of the A/D converter (ADC), V_{in} is the input voltage read by the ADC, and V_{ref} is the reference voltage for the ADC, then the relationship of the input voltage to output word is:

$$ADC = \frac{V_{in} \cdot 1024}{V_{ref}}$$

V_{ref} is currently the external 3.0V V_{cc}.

Interrupt Detection

The Atmega88 can be configured to assert (hold low) the IRQ0 pin which is attached to the main board, when the logic level changes on any (or all) of the input pins. Each input pin may be configured separately to generate the interrupt from a low->hi transition, a hi->low transition, or both. The pin (or pins) that generated the interrupt may be queried via the SPI bus from the main board.

EEPROM Access

Any byte in the lower 256 bytes of EEPROM may be read or written, one byte at a time.

I/O pin Manipulation

I/O pins D0 through D3 can be set as either an output or input. The high current driver pins, H0 to H3, can only be used as an output. If configured as an output, the pin may be set hi, low, or toggled to its opposite state.

Register Control

All the Atmega88 special function registers (SFRs) can be manipulated directly. When writing, the written value may used to set the register value, or it may be used as a mask. As a mask, it may be used to set or clear the bits of the SFR.

Memory

Any flash location may be read.

Miscellaneous Functions

There are several miscellaneous functions that are used for administration and testing. They include fetching a version number, setting the standalone ADC scale and test modes, and returning some aspects of the internal state of the firmware.

The A4 and A5 pins are not on the I/O header but may be used for A/D conversion. The voltage reference, input scale, and pin number may be selected. Each reading is a one-shot; continuous readings are not supported.

Federal Communications Commission Compliance

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try and correct the interference by one or more of the following measures: Reorient or locate the receiving antenna. Increase the separation between the equipment and receiver. Connect the equipment into an outlet on a circuit different from that to which the receiver is connected. Consult the dealer or an experienced radio/TV technician for help.

The Sun SPOTs are supplied with a shielded USB cable. Operation with a non-shielded cable could cause the Sun SPOTs to not be in compliance with the FCC approval for this equipment. The antenna used with this transmitter must not be co-located or operated in conjunction with any other antenna or transmitter; to do so could cause the Sun SPOTs to not be in compliance with the FCC approval for this equipment. Any modifications to the Sun SPOTs themselves, unless expressly approved, could void your authority to operate this equipment..

FCC Declaration of Compliance:

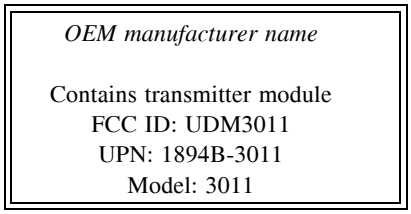
Responsible Party:
Sun Microsystems, Inc.
4150 Network Circle
Santa Clara, CA 95054
Phone: US 1-800-555-9786; International 1-650-960-1300

Products:
SLS-E5-XXXX
where “X” is any alphanumeric character or a blank.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following conditions: this device may not cause harmful interference and this device must accept any interference received, including interference that may cause undesired operation.

This device can be used as is (stand-alone) or as a module (part of a final host product). If the device will be used a module these rules must be followed:

1. **Integrator must place a label outside their product similar to the example shown**



2. **Caution: Exposure to Radio Frequency Radiation.**

   To comply with FCC RF exposure compliance requirements, a separation distance of at least 20 cm must be maintained between the antenna of this device and all persons. This device must not be co-located or operating in conjunction with any other antenna or transmitter.

   Module 3011 and antenna tested with must be integrated in the end product in such a way that the end user cannot access the either the module, cables or antennas.

   The installer of this radio equipment must ensure that the antenna is located or pointed such that it does not emit RF field in excess of Health Canada limits for the general population; consult Safety Code 6, obtainable from Health Canada's website `www.hc-sc.gc.ca/rpb`.